(a) A diagram illustrating the states and transitions of a memory device. States include 00, 01, 10, and 11, with transitions labeled as read and verify latency (t1) and programming pulse width (t2).

(b) A graph showing the resistance (Ω) of the device over the number of pulses. The resistance drops as more pulses are applied, with specific states marked as 10k, 100k, and 1M. The progression time (τ) is noted to be proportional to the resistance (RC).