SoC Design Flow

Algorithm

- Specs
- System Functional Executable Model
- Functional Simulation
- DUT Hardware
- Functional untimed/timed
- HW/SW Partitioning
- DUT Software
- Transactional Co-simulation
- Software Test pattern
- Other hardware such as Processor and memory
- Other software such as driver, OS, and API

Architecture

- SystemC
  - Transactional
  - Behavioral
  - BCA
  - Co-simulation on VM with ISS
  - Software Object code
- Formal Verification
- Timing Analysis

Implementation

- VHDL/Verilog
  - RTL
  - Gate Level Netlist
  - Co-simulation On Physical board
  - Physical Implementation
  - Layout Verification
  - Co-simulation On Physical board
  - Verilog Gate Level Netlist