W/L = 0.3x3μm/0.5μm

Drain Current $I_d(\mu A/\mu m)$ vs. Gate Voltage $V_g$ (V)

- $V_d = -0.3V$
- $V_d = -3V$

DIQL = 0.8mV/V
$I_{on}/I_{off} = 3.89 \times 10^8$

SS = 100mV/dec

(b) P-type Raised S/D JL-TFT

W/L = 0.3x3/0.5
$|V_g - V_{th}| = 1,3,5V$