PDP of CNTFET ($t_{node} = 45$ nm, $t_{sub} = 500$ nm)

![3D graph showing the Power Delay Product (PDP) for different logic gates and interconnect lengths. The graph visualizes the relationship between interconnect length and logic gate type, with the Power Delay Product (PDP) expressed in joules ($J$) and interconnect length in micrometers ($\mu$m).]