Fig. 9 (a) Schematic illustration of a nanotetrapod transistor with a 300 nm-thick ferroelectric dielectric under testing with STM tips. The source (S) and drain (D) electrodes are patterned Pt layer. (b) Typical TEM image of the multiarmed CdS nanorods used in this study. (c) The enlarged micrograph of a single CdS nanotetrapod. (d) SEM image of a single CdS nanotetrapod device. (e) In situ SEM image of two STM tips (shown in white) probing on a testing device.