Fig. 4 (a) Schematic circuit diagram of an In$_2$O$_3$ nanowire FeFETs. (b) Characteristics of the PZT-gated In$_2$O$_3$ NW transistor with $V_{DS} = -0.1$ V showing pronounced hysteresis. “1” and “0” denote two states at $V_G = 0$ V for the memory operation.