**Fig. 13** Scheme of the fabrication of the two top-gated FeFETs assembled on a single nanotube. (a) A CNT-FET fortuitously composed of an individual nanotube. (b) Coating of amorphous ferroelectric at room temperature onto the top of CNT-FET by using PLD. (c) After annealing, double top electrodes (G1 and G2) made of Pt were patterned in series onto the deposited ferroelectric films. (d) SEM image of the double-top-gated CNT-FeFET memory. (e) The schematic sequential chart for G1/G2 and the programming of the two top-gated CNT-FeFET memory.